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Compiler-based **cache line optimization** - US Patent 6564297

Cache line optimization involves computing where **cache** misses are in a control flow ...

IBM, "Selective Prefetching Based on Miss Latency" **IBM** TDB, vol. ...

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have influenced **selective optimization** technology in today's virtual show that the order of fields within a **cache line** can impact performance because ...

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US5668972 Method and system for efficient miss sequence **cache line** ... US5682491

Selective processing and routing of results among processors controlled by ...

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An **optimization** algorithm. 1. loop permutation to improve general reuse. =.) need **cache line** size. 2. tile loops to reuse **cache** lines ...

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A system employing **selective optimization** requires three. basic components: Franz

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Interesting Computer Architecture Patents -- Mark Smotherman

(**IBM**), "Cache memory architecture with decoding"; US 5442760 (1995) Rustad, et al. ...

cache line directly connected to specific functional unit" ...

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Reality-based optimization

10 W. W. Hwu , P. P. Chang, Achieving high instruction **cache** performance with an ...

based on profile propagation and **selective** profile collection, 2001 ...

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AIX 5L with IBM XL Compilers SPEC CPU Flags

This level of **optimization** will increase the compiler's memory usage and compile Set a

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